



PATENT APPLICATION  
Docket No. 9903-040  
Client No. S01US022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Hyung-Jik Byun and Kyu-Jin Lee

Serial No. 10/053,278 Examiner: Stoner, Kiley Shawn

Confirmation No. 1314

Filed: January 16, 2002 Art Unit: 1725

For: SEMICONDUCTOR CHIP PACKAGE COMPRISING  
ENHANCED PADS

Mail Stop Issue fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**TRANSMITTAL LETTER**

Enclosed for filing in the above-referenced application are the following:

- Applicant's Comments on Examiner's Statement of Reason for Allowance  
Publication and Issue Fee
- In connection with issuance of a patent:
  - Supplemental Declaration  PTO Form 85B
- PTO Form 2038 authorizing credit card payment of \$1630.00, issue fee  
(\$1330.00) and publication fee (\$300.00) is enclosed.
- Any deficiency or overpayment should be charged or credited to deposit  
account number 13-1703.

**Customer No. 20575**

Respectfully submitted,

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Date: January 9, 2004

Adrienne Chocholak



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**APPLICANT'S COMMENTS ON EXAMINER'S STATEMENT OF REASONS  
FOR ALLOWANCE**

Applicant submits that the prior art alone or in combination does not teach a substrate for forming a ball grid array (BGA) package, comprising:

a substrate having a top surface and a bottom surface, the bottom surface having ball pads; and  
a plurality of enhanced pads formed on the bottom surface, each enhanced pad having one or more dummy pads coupled to one or more dummy patterns,

wherein said enhanced pads comprise a first enhanced pad, and wherein the first enhanced pad comprises a ball pad, a plurality of dummy pads, and a plurality of dummy patterns configured to connect said ball pad to said dummy pads, as recited in allowed claim 1.

Applicant submits that the prior art alone or in combination does not teach a semiconductor chip package comprising:

a substrate having a top surface and a bottom surface, the bottom surface having ball pads;

a plurality of enhanced pads formed on the bottom surface, each enhanced pad having one or more dummy pads coupled to one or more dummy patterns;

a semiconductor chip mounted on and electrically connected to the top surface of the substrate,

wherein said enhanced pads comprise a ball pad, a plurality of dummy pads, and a plurality of dummy patterns configured to connect said ball pad to said dummy pads, as recited in allowed claim 4.

Applicant submits that the prior art alone or in combination does not teach a method of forming a substrate for a BGA package, comprising:

arranging ball pads on a bottom surface of the substrate;

arranging a plurality of enhanced pads on the bottom surface of the substrate, said enhanced pads comprising at least one dummy pad coupled to at least one dummy pattern,

wherein said enhanced pads comprise a ball pad, a plurality of dummy pads, and a plurality of dummy patterns configured to connect said ball pad to said dummy pads, as recited in allowed claim 19.

Applicant submits that the prior art alone or in combination does not teach the method of attaching a semiconductor package to a board, comprising:

preparing a board by exposing ball lands and enhanced lands from a photo solder resist (PSR) layer;

applying a mask, having openings corresponding to the ball lands and the enhanced lands, to the board;

applying a solder paste on the ball lands and the enhanced lands;

removing the mask;

attaching solder balls to ball pads and enhanced pads of a substrate; and

attaching the substrate to the board with the solder balls and the solder paste using a solder reflow process,

wherein each of said enhanced pads comprises one or more dummy pads coupled to one or more dummy patterns, as recited in allowed claim 23.

Applicant submits that the prior art alone or in combination does not teach a semiconductor chip package comprising:

a substrate having a top surface and a bottom surface, the bottom surface having ball pads;

a plurality of enhanced pads formed on the bottom surface; and

a semiconductor chip mounted on and electrically connected to the top surface of the substrate,

wherein said enhanced pads comprise a ball pad, a dummy pad, and a dummy pattern configured to connect said ball pad to said dummy pad, as recited in allowed claim

26.

Applicant submits that the prior art alone or in combination does not teach a method of forming a substrate for a BGA package, comprising:

arranging ball pads on a bottom surface of the substrate;

arranging a plurality of enhanced pads on the bottom surface of the substrate, said enhanced pads comprising a ball pad, a dummy pad, and a dummy pattern configured to connect said ball pad to said dummy pad, as recited in allowed claim

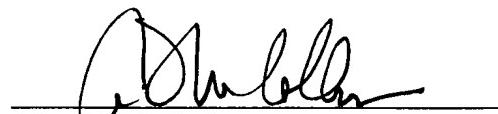
27.

The remaining claims further distinguish over the prior art.

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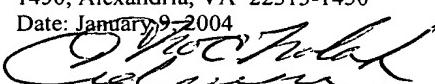
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